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Intelligent Automation Incorporated

Coherent distributed radar for high-resolution through-wall imaging

SBIR Phase I Progress Report 7

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Summary

In this performance period we performed the first measurements with the digital synchronization transceiver hardware. We have characterized the tenability and stability of the reference clocks used to clock the transceiver's digital hardware. We have tested the ADC board, and have discovered several issues with its performance. We have completed the redesign of the ADC board to address these issues. The RF front-end is in manufacture now, and will be tested shortly. We have finalized our approach to frequency synchronization which addresses the effects of multipath and mobility. We have tested the frequency synchronization algorithm in a loopback test on the digital transceiver hardware. We are designing a final demonstration using the synchronization transceiver and in-house radar- and high-precision hardware.

1.0 INTRODUCTION

In this report we discuss progress in hardware design, synchronization algorithm, and definition of the final demonstration.

1.1 Synchronization algorithm

We have completed Matlab simulations of the estimated the performance of frequency estimation algorithm under varying SNR through simulations. We have also tested this algorithm using data collected on the digital transceiver in a loopback test, i.e. the transceiver transmits a tone and receives it simultaneously. For relevant achievable SNR values, and mobility consistent with hand-held radars, the accuracy of the frequency estimation algorithm is comparable to the tenability and stability of the reference clocks. This means that frequency estimation may not be needed during operation in the field more than once a day. To reduce the effort in implementing the frequency synchronization algorithm, we have decided to implement it outside the FPGA, in an external processor in floating point precision.

For time synchronization, we are now completing Matlab simulations of our synchronization of multiple moving nodes, in a multi-tap multipath channel. We have also started implementation of the time offset estimation algorithm in the digital hardware.

1.2 Hardware design

Part of the hardware design and implementation was supported by other efforts at IAI using the same hardware design. The RF layout was sent out for manufacture, and will be tested in October, 2010. The ADC board testing was completed, and has prompted a redesign to address problems with the analog input circuit, specifically level shifters. The redesign has been sent out for manufacture and the redesigned hardware testing will be completed in October, 2010.

We have extensively tested the stability and tenability of the reference clocks used for the synchronization transceivers. We have developed an automated (using LabView) test set-up to accurately measure the frequency offset between two clocks, and used it to characterize the stability of the clocks over time scales varying from 0.05s to several hours. We have also studied the effect of power supply stability and accuracy on clock frequency accuracy and stability. We are using these results to select proper power supplies and tuning circuits to tune the clocks in the field.

1.3 Preparation for final demonstration

We have accelerated the preparation of the final demonstration. We are redesigning a previously developed through-wall radar to be interfaced to our synchronization hardware. We are also planning for manufacture of a second unit of this radar, so that we can demonstrate the improved cross range resolution afforded by using two separated, tightly synchronized radars.

3.0 CONCLUSIONS AND WORK PLANNED FOR NEXT REPORTING PERIOD

The next reporting period will focus on implementation of the time offset estimation algorithm in the digital hardware, characterization and testing of the RF hardware, specifically the achieved noise figure, and ability to accurately measure hardware delays. We will complete the definition of the final demonstration and present a schedule of activities remaining in preparation for the demonstration.

3.0 REFERENCES

None.

4.0 LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS